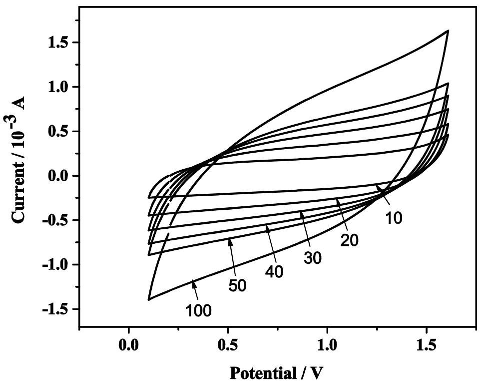

Fig. 5 Cyclic voltammograms obtained by varying the scan rate of cycling within the potential window 0.1 V – 1.6 V at room temperature

reactions. Low scan rate cyclic voltammograms show conventional parallelogram shape indicating that charge discharge takes place in the synchronous region where the rate of reactions are equal. Due to the inability of the slow fraction of capacitive states to keep up with the applied voltage perturbation, shape of cyclic voltammograms becomes biconvex (Fletcher *et al*. 2014). Further, Hashmi *et al* have reported that some shape deviations could be observed with higher scan rates probably due to higher ESR values (Hashmi *et al*. 2007). Amount of deviation would have been controlled by high conducting GPE.

When the scan rates were increased, C_s values showed a decreasing trend as reported in literature (Wang *et al*. 2013). For proper and complete charge storage, there should be ample time for the respective mechanism to take place. At slow scan rates, charges can go deeper into the electrodes. This contributes for higher C_s. In addition, at high scan rates, energy loss increases and as a result, charge storage becomes weak. This leads to decrease in specific capacity. But, very slow scan rates on the other hand can give rise to unwanted reactions which might disturb the proper operation of EDLCs. The scan rate of 10 mV/s was selected to be used for continuous cycling.

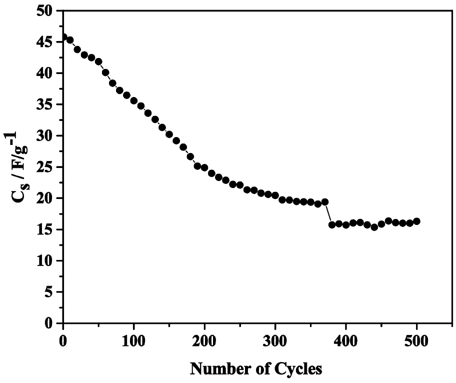

Fig. 6 Variation of single electrode specific capacity (C_s) with cycle number at the scan rate of 10 mV/s within the potential window 0.1 V – 1.6 V at room temperature

Fig 6 shows the variation of C_s with cycle number. C_s variation from about 48 F/g to 16 F/g occurred while cycling for 500 cycles.

The rate of decrease is fast during first 300 cycles. After that, it had reached a nearly steady state. At the beginning, the interfacial contacts may not be mature enough to take part in the charge storage process. Upon continuous cycling, the setup may reach maturity resulting somewhat stable performance. It is a well-accepted fact that, from the total capacity of an EDLCS, 10-20% is due o redox capacitance. It is a faradaic process involving electron transfer. If redox capacitance was present, peaks should appear in voltammograms (Liew and Ramesh 2014). But, in none of the case, that behavior could not be observed. This indicates that the charge storage mechanism of the present EDLCs are purely electrostatic giving rise to pure capacitive behavior.

3.3 Galvanostatic Charge Discharge (GCD) Test

Fig. 7 shows several initial GCD curves and Fig. 8 represents the variation of single electrode discharge capacity (C_d) with cycle number.

As per Fig. 7, it is seen the presence of ohmic loss across the internal resistance which is called as equivalent series resistance (ESR) with the initial sudden jump/drop of potential in charge/

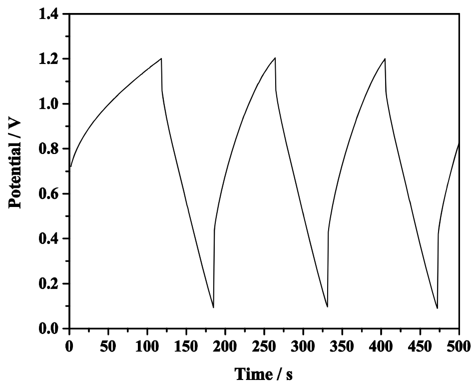

Fig. 7 Initial charge discharge profile obtained under a constant current of 2×10^{-4} A at room temperature

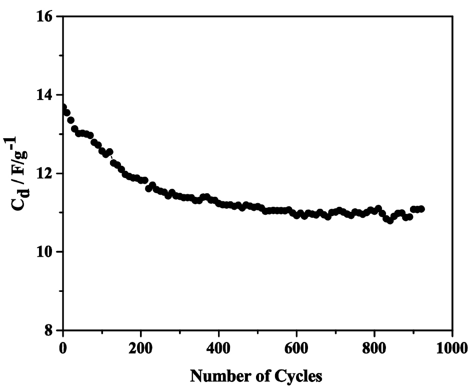

Fig. 8 Variation of single electrode specific discharge e capacity (C_d) with cycle number

discharge stages (Pandey *et al*. 2013). For 900 cycles, C_d has changed from 13.68 F/g to 11.01 F/g which is not a fast decrease. Only up to about 200 cycles, the decrease rate is quite faster. Then, C_d becomes more or less stable. During initial cycles, the fast capacity fade may result due to two reasons as suggested by Pandey *et al*. namely i. consumtion of some charges for irreversible reactions ii. possibility of permanent filling of some micro pores of AC (Pandey *et al*. 2010).

However, capacitance values obtained by different techniques are not comparable to each other due to mismatch of time scales of measurements. As an example, if the time durations taken for charge and discharge processes in CV and GCD tests are not equal, the results may be different. Anyway, different methodologies should be used to evaluate the performance under numerous conditions such as scan arte, potential window of cycling and frequency range.

4. Conclusions

All solid state EDLCs were prepared using a composite electrode having NG, AC and PVdF with a GPE. NG blends well with AC and results the optimum C_s of 14.65 F/g for the composition of 50 NG and 40 AC. Above and below 50, C_s is somewhat lower showcasing the fact that NG plays a role on determining C_s. Continuous cycling at the potential window of 0.1 to 1.6 V and the scan rate of 10 mV/s evidenced the ability of the EDLC to withstand for continuous operation. But, further work is needed to improve the performance. Higher value of relaxation time is an evidence for the slow charge transfer in the device. This should be expedited. C_d did not change very fast which is a satisfactory feature for using the EDLC for applications. The most appealing feature of this study is exploring the suitability of Sri Lankan NG for super capacitor applications.

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