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Dislocations as native nanostructures - electronic properties

Manfred Reiche[*1], Martin Kittler[2,3], Hartmut Uebensee[4], Eckhard Pippel[1] and Sigrid Hopfe[1]

[1]*Max Planck Institute of Microstructure Physics, Weinberg 2, D-06120 Halle, Germany*
[2]*IHP Microelectronics, Im Technologiepark 25, D-15236 Frankfurt (Oder), Germany*
[3]*IHP/BTU Joint Lab, K.-Wachsmann-Allee 1, D-03046 Cottbus, Germany*
[4]*CIS Research Institute of Microsensorics and Photovoltaics, K.-Zuse-Str. 14, D-99099 Erfurt, Germany*

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Abstract. Dislocations are basic crystal defects and represent one-dimensional native nanostructures embedded in a perfect crystalline matrix. Their structure is predefined by crystal symmetry. Two-dimensional, self-organized arrays of such nanostructures are realized reproducibly using specific preparation conditions (semiconductor wafer direct bonding). This technique allows separating dislocations up to a few hundred nanometers which enables electrical measurements of only a few, or, in the ideal case, of an individual dislocation. Electrical properties of dislocations in silicon were measured using MOSFETs as test structures. It is shown that an increase of the drain current results for nMOSFETs which is caused by a high concentration of electrons on dislocations in p-type material. The number of electrons on a dislocation is estimated from device simulations. This leads to the conclusion that metallic-like conduction exists along dislocations in this material caused by a one-dimensional carrier confinement. On the other hand, measurements of pMOSFETs prepared in n-type silicon proved the dominant transport of holes along dislocations. The experimentally measured increase of the drain current, however, is here not only caused by an higher hole concentration on these defects but also by an increasing hole mobility along dislocations. All the data proved for the first time the ambipolar behavior of dislocations in silicon. Dislocations in p-type Si form efficient one-dimensional channels for electrons, while dislocations in n-type material cause one-dimensional channels for holes.

Keywords: dislocations; one-dimensional nanostructures; electronic properties; MOSFETs; semiconductor wafer bonding

1. Introduction

Dislocations are elementary crystal defects. The structure and electronic properties of dislocations in silicon have been studied for more than five decades (Alexander and Teichler 1991, Reiche and Kittler 2011). A large number of models of the structure of dislocation cores were proposed by computer simulations. An experimental verification, however, is missing up to now. Moreover, most of the techniques applied to characterize electronic properties require high densities of dislocations. Analyzing such large numbers of these defects implies that interactions

*Corresponding author, Ph.D., E-mail: reiche@mpi-halle.de

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between individual defects and interactions with other defects (point defects) are simultaneously recorded. Therefore the optimum conditions to characterize electronic properties of these defects are measurements on individual dislocations. A way to realize defined arrangements of dislocations and experimental measurements of only a few dislocations are demonstrated in the present paper.

It is generally believed that dislocations result in significant effects on device parameters of electronic circuits. A detrimental effect was proved if dislocations are generated in an uncontrolled manner by high-temperature treatments during processing (Ravi 1981). Therefore they are avoided. A beneficial effect, however, is obtained if dislocations are generated far from device active areas. This effect is used, for instance, as internal gettering of impurities. Furthermore, dislocations may be also considered as one-dimensional native nanostructures with extraordinary optical and electronic properties (Kittler *et al*. 2007). For instance, an increase of the electrical conductivity of about four orders of magnitude compared to that of bulk silicon was measured along dislocations (Reiche *et al*. 2010). If these distinguished properties are usable, devices (MOSFETs) with dimensions below 10 nm and high *on currents* (I_{ON}) are feasible. Their realization, however, requires the defined and reproducible generation of dislocation arrays.

2. Dislocations in Si

Silicon crystallizes in the cubic diamond structure (space group Fd3m). The lattice constant is *a* = 0.543 nm. The glide plane is {111} and perfect dislocations have Burgers vectors of the type $\mathbf{b}$ = a/2<110>. Two types of perfect dislocations are known in the diamond lattice: pure screw dislocations and the so-called 60° dislocations, where the Burgers vectors are inclined at an angle of 60° to the dislocation line (Hornstra 1958). Caused by the diamond structure, which corresponds to two face-centered cubic (fcc) lattices displaced by (¼, ¼, ¼), two distinct sets of {111} lattice planes exist, the closely spaced glide subset and the widely spaced shuffle subset (Hirth and Lothe 1982). There was a long controversial discussion about the dominant dislocation type in the diamond structure. Early investigations suggest the presence of dislocations in the shuffle set because movement through one repeat distance on a shuffle plane breaks one covalent bond per atomic length of dislocation (Seitz 1952), while an equivalent step on a glide plane involves the breaking of three bonds (Amelinckx 1982). On the other hand, applications of electron microscopy, especially of the weak-beam technique, have particularly shown that dislocations in silicon are in general dissociated and glide in this extended configuration (Gomez and Hirsch 1977, Ray and Cockayne 1971). Today, it is generally assumed that most of the dislocations in silicon, especially after plastic deformation, belong to the glide set (Alexander 1986, Duesbery and Joas 1996).

The dissociation of a 60° dislocation results in a 30° partial and a 90° partial dislocation, while a screw dislocation dissociates into two 30° partials. The dissociation follows the reaction (Marklund 1979)

$$\mathbf{b} \rightarrow \mathbf{b}_1 + \mathbf{b}_2 \tag{1}$$

where in the case of a 60° dislocation

$$\mathbf{b} = \frac{a}{2}[011] \qquad \mathbf{b}_1 = \frac{a}{6}[121] \qquad \mathbf{b}_2 = \frac{a}{6}\left[\bar{1}11\right] \tag{2a}$$

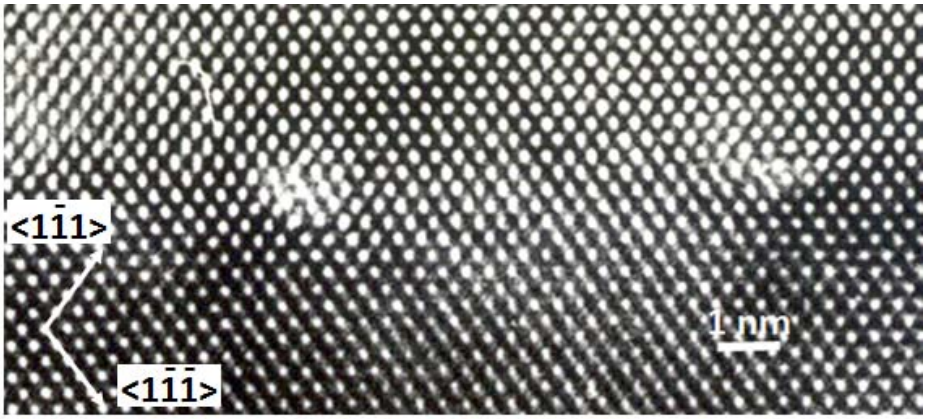

Fig. 1 Cross-section image ({110} plane) of two screw dislocations in silicon. The diameter of the dislocation cores is about 1 nm. High-resolution electron microscope (HREM) image

and for a screw dislocation

$$\mathbf{b} = \frac{a}{2}[011] \qquad \mathbf{b}_1 = \frac{a}{6}[121] \qquad \mathbf{b}_2 = \frac{a}{6}\left[2\bar{1}1\right] \tag{2b}$$

holds.

Numerous models have been proposed about the structure of dislocations (Reiche and Kittler 2011). Because dislocations are line defects, a structural disorder exists only in one dimension. This so-called dislocation core may be a few micrometers in length but has a diameter of only 1 nm (Fig. 1). First models of perfect dislocations assumed dangling bonds in their core (Hornstra 1958). Experimental data, however, obtained mainly by electron paramagnetic resonance (EPR) spectroscopy refer to a low density of such dangling bonds (Alexander and Teichler 1991). Therefore different models of the reconstruction of perfect and partial dislocations have been proposed by computer simulation (Bulatov and Cai 2006).

3. Fabrication of defined dislocation arrangements

Most of the studies of optical and electronic properties of dislocations used plastically deformed silicon in order to achieve defined dislocation arrangements and a high density of dislocations to attain the detection limit of the methods applied (Alexander and Teichler 1991, Kveder *et al*. 2001, Schroter and Cerva 2002). Plastic deformation, however, results also in a large number of point defects and defect reactions making it sometimes difficult to interpret experimental data (Alexander and Teichler 1991). In order to avoid interactions between dislocations or between dislocations and other defects, methods are required allowing the realization and analyses of only a few dislocations or, in the ideal case, of an individual dislocation. A method to realize defined dislocation arrangements in a reproducible way is semiconductor wafer direct bonding (SWDB) originally developed to produce silicon on insulator (SOI) substrates and three-dimensional micro-electromechanical systems (MEMS) (Tong and Gosele 1999). If two wafers are joined together without any interface layers, a two-dimensional

dislocation network is obtained analogous to early experiments on bicrystals (Thibault-Desseaux *et al*. 1989). For bicrystals a Czochralski growth process is required allowing only the formation of specific grain boundaries such as Σ = 9 (rotation 38°56´17´´, boundary plane (122), common [011] axis), Σ = 13 (rotation 26°37´12´´, boundary plane (510), common [001] axis), and Σ = 25 large angle grain boundaries (rotation 16°15´36´´, boundary plane (710), common [001] axis) (Aubert and Bacmann 1987). Semiconductor wafer direct bonding, on the other hand, uses commercially available wafers making it possible to realize any grain boundary. Especially small angle grain boundaries having rotational angles $\alpha << 1°$ are of interest allowing dislocation distances of a few hundred nanometers. Applying state of the art techniques for preparation and analyses individual or a small number of dislocations can be characterized.

Semiconductor wafer direct bonding (SWDB), or fusion bonding, describes a method to join two or more mirror-polished semiconductor wafers at room temperature without the addition of any glue or external forces. The most common technique is the bonding of oxidized (hydrophilic) wafers. When, as in the case of silicon, the oxide layer is removed with HF, a hydrophobic surface with unique properties is obtained, i.e., having a good resistance to chemical attacks and a low surface recombination velocity. This means a surface with a very low density of surface states. The removing of the oxide results that two silicon crystal lattices are in contact and Si-Si bonds formed via the interface. Crystal defects (dislocations) are generated and form a two-dimensional network in order to match both crystal lattices. The structure of the dislocation network depends on the surface orientation of both wafers. Bonding of Si(100) wafers, for instance, cause a Σ = 1 (100) small angle grain boundary characterized by a square-like mesh of screw dislocations expected from theory (Bollmann 1970). An example is shown in Fig. 2(a). These dislocations are caused by the rotational misfit (twist) between both crystal lattices. There is, however, an additional tilt component caused by the deviation on the [001] axis of real wafers (cut-off). The tilt component is compensated by a periodic array of 60° dislocations. The spacing between dislocations *S* in both networks are indirectly proportional to the misalignment angle and are given by

$$S_{twist} = \frac{a}{2\sqrt{2} \cdot \sin\dfrac{\alpha_{twist}}{2}} \tag{3}$$

for the screw dislocation network. On the other hand, the relation between dislocation distance and tilt angle of the network formed by 60°-dislocations follows as

$$S_{tilt} = \frac{a}{2 \cdot \tan \alpha_{tilt}} \tag{4}$$

In both equations *a* means the lattice constant and α_{twist} and α_{tilt} are the angles of misorientation of the twist and tilt component, respectively.

Reactions between screw and 60° dislocations are occurred during additional annealing treatments after the initial bonding. Depending on the temperature, mixed dislocations may be formed having different Burger vector components. Besides this reaction, also dissociation reactions of screw dislocations are dominant processes even at annealing above 1100°C. Fig. 2(b) shows one set of screw dislocations of the network in Fig. 2(a) under weak-beam conditions. A splitting of the dislocation lines can be seen indicating the dissociation of perfect screw dislocations. The dissociation follows Eq. (1) and result in the formation of two 30° partial dislo-

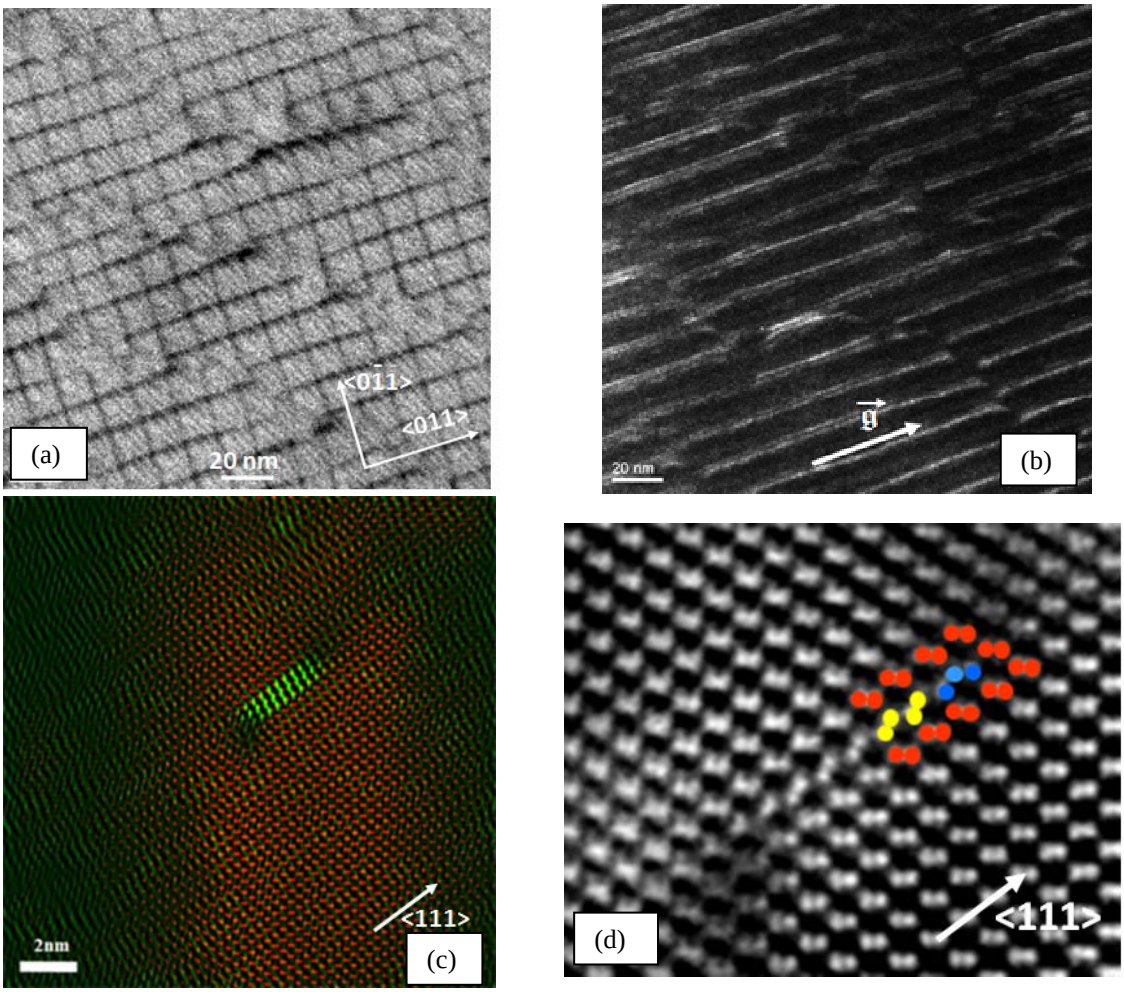

Fig. 2 Scanning transmission electron microscope (STEM) plan-view image of a screw dislocation network formed by wafer bonding of Si(100) wafers (a). Weak beam dark field (WBDF) image of one set of dislocations (b). The image was recorded using the weak $\vec{g}[044]$ reflection and by excitation of the $[0\bar{2}\bar{2}]$ reflection. HAADF-STEM image of a dissociated screw dislocation (c). The image was color coded for clearness. A part of the defect is shown at higher magnification in (d). Red dots characterize dumbbells of the (undisturbed) Si matrix, while blue and yellow dots are dumbbells at the partial dislocation and stacking fault, respectively. Each dumbbell characterizes two Si columns separated by 0.136 nm in the undisturbed silicon lattice. Samples with <100> orientation were used for Figs. (a) and (b), while Figs. (c) and (d) were produced from <110> oriented cross sections of the same dislocation network

cations according to Eq. (2b). The distance between both partial dislocations is about 2 nm.

High-resolution electron microscopy (HREM) and high-angle annular dark field (HAADF) imaging obtain more details of these defects. Fig. 2(c) shows a color-coded HAADF image of a dissociated screw dislocation with the stacking fault between both 30° partial dislocations. The size of the stacking fault is 2 nm which corresponds to the data of weak-beam analysis. At higher

magnification silicon dumbbells are clearly resolved in the HAADF images of Si[110], in which two Si columns are separated by 0.136 nm (Fig. 2(d)). The changes of the symmetry of the dumbbells are cleary seen at the partial dislocation and stacking fault. The different colors in the figure characterize these changes. Further investigations in combination with computer simulations are required to explain the structure of the partial dislocations and stacking fault.

4. Electronic properties of dislocations

4.1 Properties of dislocations in bonded interfaces

Dislocations in the interface of bonded wafers possess numerous remarkable properties which may be used for different applications (Kittler and Reiche 2009, Kittler *et al*. 2007). The electrical properties of bonded hydrophobic silicon wafers were studied for the first time by Bengtsson *et al*. (1992). The measurement of the capacitance-voltage (CV) characteristics on bonded unipolar wafers were interpreted on the assumption of two distributions of interface states, one of acceptors and one of donors, causing a potential barrier at the bonded interface. The origin of the interface states was assumed to be impurities and crystal defects. More recent analyses by electron beam induced current (EBIC) technique proved barrier heights generally smaller than 100 meV for different types of bonded hydrophobic wafers (Yu *et al*. 2006). The concentration of deep levels along the interface was determined to be a few 10^5 per cm. Low concentrations of deep levels at the interface are also the reason for low dark currents, an improved CV-characteristics, and fast rise times of pin-diodes prepared on bonded hydrophobic wafers (Reiche *et al*. 2002).

One-dimensional conductive channels formed by defects in solar silicon have already been demonstrated (Kittler *et al*. 2008). An analysis of dislocation networks in Si revealed a similar feature. The EBIC micrograph in Fig. 3a shows a horizontal bright line extending from the Schottky contact on the upper right corner over a large distance. This demonstrates the transport of minority carriers along the dislocation network towards the collecting Schottky barrier. The transport of minority carriers over distances of more than 10 mm has been observed (Kittler *et al*. 2008).

4.2 Analyses of individual dislocations

The study of individual dislocations or small numbers of dislocations is an important issue because all of the interactions between defects can be eliminated. This result in more precise data about the electronic structure of dislocations and, combining these investigations with microscopic observations, conclusions about the correlation between the structure and properties of dislocations are derived. A combination of bonded wafer pairs with preparation methods to separate individual dislocations or a small number of dislocations allow such experiments. Twist angles between two bonded Si wafers below 0.1° results in dislocation distances of more than 100 nm (Eqs. (3), (4)). Using photolithography and etching techniques, individual dislocations can be separated and measured.

Diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs) were prepared on such bonded wafers. In order to avoid the effect of bulk material, dislocation networks were realized in SOI wafers having only a thin device layer. The substrates were prepared by hydrophobic wafer bonding of commercially available SOI wafers. After dipping in diluted HF the

(a) (b)

Fig. 3 Formation of a conducting channel along the dislocation network in the interface of a bonded Si wafer pair (a). EBIC micrograph. Sketch of the experimental setup (b)

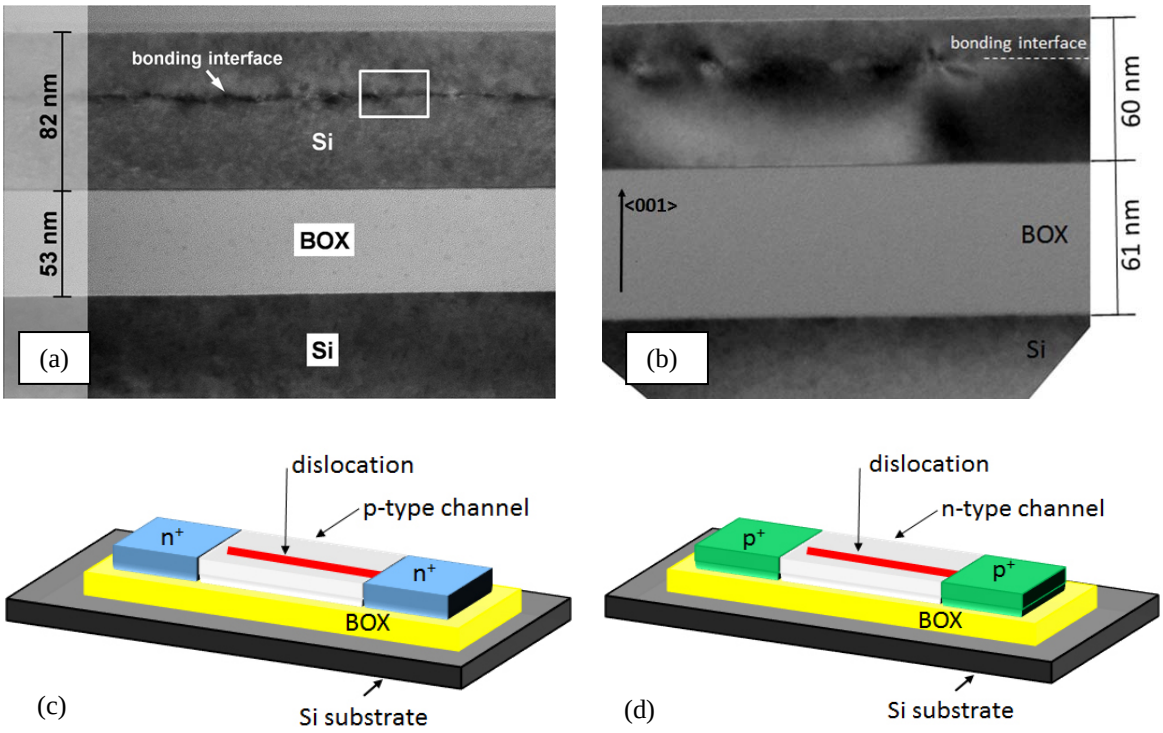

Fig. 4 TEM cross-section images of SOI substrates with dislocation networks in a *p*-type (a) and an *n*-type device layer (b). The dislocation distance is about 15 nm in both cases corresponding to a twist angle of about 0.7°. Cartoon of an nMOSFET prepared on *p*-type material (c) and a pMOSFET prepared on *n*-type material (c). Because dislocations are parallel to <110>-directions in Si, they are parallel to the channel and source and drain form electrical contacts. Note that the gate electrodes are not shown in the scheme for clearness

wafers were bonded in an atmospheric environment. Various twist angles in the range of $0.01° < \alpha_{twist} < 0.65°$ were realized. The bonded wafer pairs were annealed at temperatures between 1000°C and 1100°C for 4 hours in nitrogen. Finally one of the handle wafers was removed by a combination of mechanical grinding and chemical etching (spin etching) followed by chemical

etching of the oxide layer. This process results in SOI wafers having 2-dimensional dislocation networks in their thin device layers (Fig. 4(a), (b)). SOI MOSFETs were prepared on such substrates using lithographic techniques and reactive ion etching (RIE). In order to avoid any dopant segregation on dislocations during channel implantations, initial *p*-type material was used for nMOSFETs, while *n*-type material was applied for pMOSFETs.

The channel region was defined first. Because dislocations are parallel to <110>- directions in Si, they are parallel to the channel (Fig. 4(c), (d)). In order to study the effect of the dislocation density, channel width and length, respectively, were varied between 1 μm and 10 μm. Source and drain contacts were formed by As^+ implantation (5 keV, $1{\cdot}10^{15}cm^{-2}$) combined with a RTA step (950°C, 60 sec.) for nMOSFETs. For pMOSFETs, B^+ implantations (3keV, $1{\cdot}10^{15}$ cm^{-2}) and spike-annealing (RTA, 1000°C, 10 sec) were applied. A thin gate oxide of about 6 nm was formed by thermal oxidation. The device gates were prepared by low-pressure chemical vapor deposition (LP-CVD) of polycrystalline silicon (100 nm thick) followed by As^+ implantation (30 keV, $1{\cdot}10^{15}cm^{-2}$ and a RTA step at 950°C for 60 sec) for nMOSFETs, or B^+ implantation (10 keV, $1{\cdot}10^{15}$ cm^{-2} and a RTA step at 1000°C for 10 sec) for pMOSFETs. Finally, contacts were formed by Al deposition and annealing at 420°C for 30 minutes in hydrogen.

In order to identify the effect of dislocations on electrical parameters of MOSFETs, reference devices were prepared without dislocations. The same SOI material was used, thinned down to equivalent device layer thickness, and processed in the same run. This allows direct comparisons of electrical measurements of devices with and without dislocations.

The I-V characteristics of nMOSFETs with and without dislocation networks in the channel are shown in Fig. 5. The thickness of the device layer was about 80 nm. The channel length is 1μm. Typical output and transfer characteristics are obtained for the reference sample without dislocations (Figs. 5 (a), (b)). The devices are characterized by a subthreshold slope S =100 mV/dec. and a threshold voltage V_T = -150 mV. The output and transfer characteristics of a device with a dislocation network in the channel are shown in Figs. 5(c) and 5(d). It can be seen that higher drain currents (I_D) are measured at the same gate (V_G) and drain (V_D) voltages, compared to devices without a dislocation network. The increase of the drain current even at very low gate voltages is about one order of magnitude. Similar results were also obtained by other authors (Ishikawa *et al.* 2006) and are ascribed to the presence of dislocations. The relatively high source-drain current even at V_G = 0V, in contrast to the reference sample, indicates the presence of charged carriers on the dislocations.

Analyses of the device data clearly proved that the number of dislocations in the channel characteristically affects the device parameter. Indications are found by measurements on devices prepared on wafers having dislocation networks with different dislocation density. Such networks are realized by varying the twist angle during the wafer bonding process. Besides devices prepared on a dislocation network with α_{twist} = 0.31° (resulting in a dislocation spacing of about 35 nm) analogous samples were prepared on a wafer having a dislocation network characterized by α_{twist} = 0.035°. Here, the dislocation spacing is about 150 nm. Using channel widths W between 1 µm and 10 µm, devices having about 660 dislocations (at a dislocation spacing of 15 nm and W = 10 μm) up to 6 dislocations per channel at a dislocation spacing of 150 nm and W = 1 μm were prepared. The $I_D - V_D$ curves of these devices show that the drain current depends on the number of dislocations in the channel. At V_D = 2 V, a drain current of $3{\cdot}10^{-3}$ A is obtained if there are only 6 dislocations in the channel. On the other hand, a value of $I_D = 2{\cdot}10^{-6}$ A is measured under the same conditions if the channel includes about 660 dislocations. If the drain current is plotted as a function of the number of dislocations, a linear relation is obtained (Reiche *et al.* 2011). It is

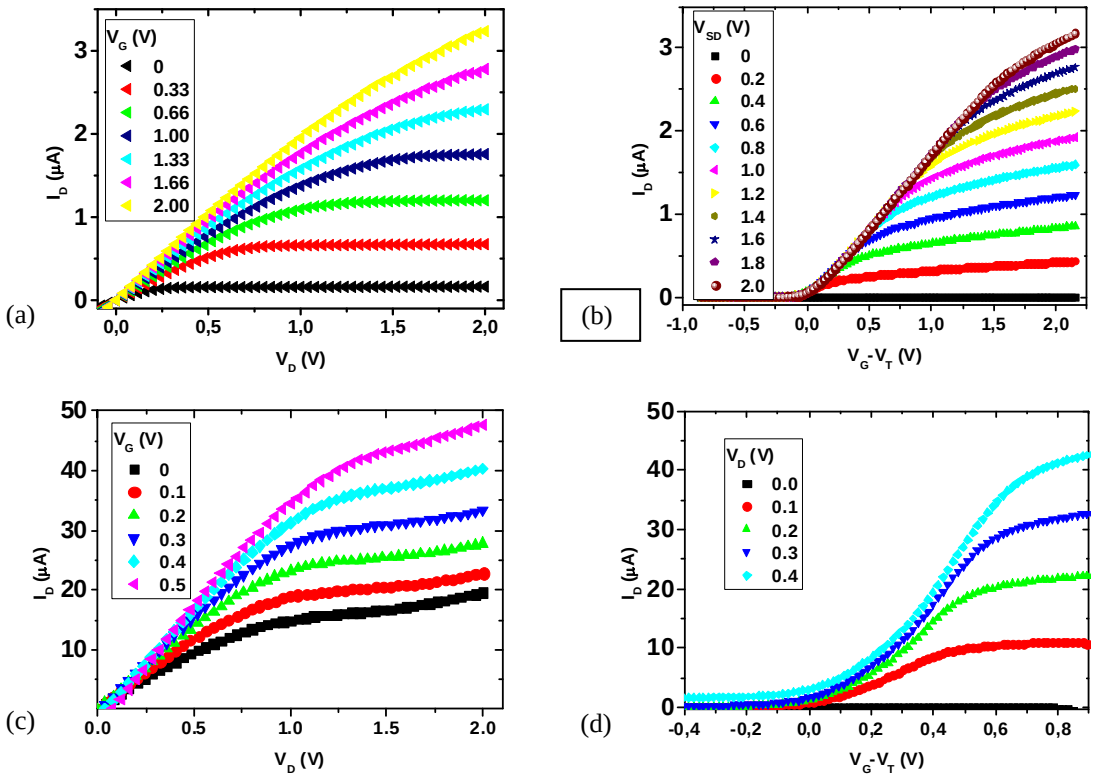

Fig. 5 Output and transfer characteristics of nMOSFETS without dislocations (a, b) and with a dislocation network (c, d). The device layer thickness was 80 nm. The channel length and width, respectively, for both devices are 1 μm. Caused by the different threshold voltages (V_T) of both devices, the gate voltage (V_G) is represented for clarity as $V_G - V_T$

shown that the drain current decreases as the number of dislocations in the channel increases. Fitting the data allows to extrapolate the current given by one dislocation of more than 10^{-2} A, which corresponds to a current density of more than 10^{12} A/cm^2.

Besides I_D also the threshold voltage (V_T) and the subthreshold swing depend on the dislocation density. Increasing the number of dislocations by a factor of 10, by increasing the channel width from 1μm to 10 μm, results in a decrease of V_T from about -400 mV down to -150 mV for nMOSFETs. An explanation could be the dependence of V_T and the subtreshold voltage shift (ΔV_T) on the effective channel length of MOSFETs (Liu *et al*. 1993). Decreasing the effective channel length results in an increase of ΔV_T. If dislocations are present in the channel, the effective channel length is defined by the number of dislocations as the effective transport channels. Therefore, reducing the number of dislocations in the channel result in an increase of V_T and ΔV_T. Furthermore, an analogous increase of the subthreshold swing is generally interpreted as thickness effect of the device layer for short channel SOI-MOSFETs and is caused by an inhomogeneous electron concentration in the layer (Rauly *et al*. 1999).

The application of MOSFETs allows not only the advantageous measurement of electronic

properties of a few dislocations but also a more detailed interpretation of the data by means of device physical principles. For instance, commercially available device simulation programs make it possible to calculate the current-voltage characteristics of MOSFETs enabling conclusions about the physical reasons behind. The ATHENA/ATLAS simulation package (Silvaco) was used (Reiche *et al*. 2013). Because dislocations represent conductive channels, they are assumed as thin *n*-type layers embedded in the 80 nm thick channel. The I_D-V_D- and I_D-V_G characteristics are calculated and compared with the experimentally measured ones by fitting the donor concentration in this thin layer. It was shown that a donor concentration of $3 \cdot 10^{18}$ cm^{-3} in the thin layer results in an increase of I_D by one order of magnitude as proved by experimental measurements. This is caused by the formation of a conductive channel along the thin (dislocation) layer already at very low drain and gate voltages. The reference transistor without dislocations, however, is characterized by an electron concentration more than one order of magnitude lower. A conductive channel is not formed under these conditions. Since the donor concentration is equal the electron concentration, the number of electrons in the 2 nm thick layer is estimated to be 6000 for $W = L = 1\ \mu$m. Furthermore, the behavior of the subtreshold slope refers to an inhomogeneous electron concentration (Reiche *et al*. 2011) which suggests that all electrons are bounded to dislocations. TEM investigations revealed that there are 30 dislocations in the channel for this specific case, which means about 200 electrons per micrometer dislocation length. This corresponds to the maximum number of electrons on a dislocation (Kveder and Kittler 2008). Assuming a homogeneous distribution along the dislocation line, the distance between free electrons on the dislocation core is about 5 nm. There is no evidence up to now about the locations of electrons on the dislocation core. The distance of about 5 nm is significantly smaller than the distance of dislocation nodes in the network (about 30 nm in this case) and means that electrons are located on straight dislocation segments. Moreover, kinks on dislocations could be a promising candidate. But only narrow kink-kink distances of about $d \cong 2b \cong 1.6$ nm are stable. Here b is the length of the Burgers vector. Larger kink-kink distances up to $d \cong 10b$ were calculated but it was shown that such wide kinks are intermediate states only. Therefore metallic conduction along dislocation lines in the *p*-type material is assumed in accordance with other authors (Labusch and Schroter 1980). It is caused by a two-dimensional carrier confinement along dislocations. The assumption of a metallic-like behaviour may explain also the occurrence of Coulomb blockades proved by low-temperature measurements at $T = 5$ K. These investigations showed a staircase-like behavior of the conductance G as a function of V_G if screw dislocations are present, while periodic oscillations of G are obtained for mixed dislocations resulting from the reaction of screw with 60° dislocations (Reiche and Kittler 2012). The distances of the Coulomb islands were calculated to be about 4 nm for screw dislocations and about 8 nm for mixed dislocations. These values are in good agreement with distances of electrons of 5 nm estimated from simulations.

4.3 Carriers on dislocations

As shown above, MOSFETs are an excellent tool to analyze electronic properties of dislocations. An excess concentration of electrons was proved for dislocations introduced in the channel of nMOSFETs. Such devices are typically produced in *p*-type silicon. A completely different behavior is obtained, if pseudo-pMOSFETs are prepared in the same *p*-type material. Then the drain current measured for such devices without dislocations (reference) is about one order of magnitude lower as for equivalent nMOSFETs. This is mainly due to the lower mobility of holes compared to that of electrons in silicon. A further reduction of I_D by a factor of 100 or

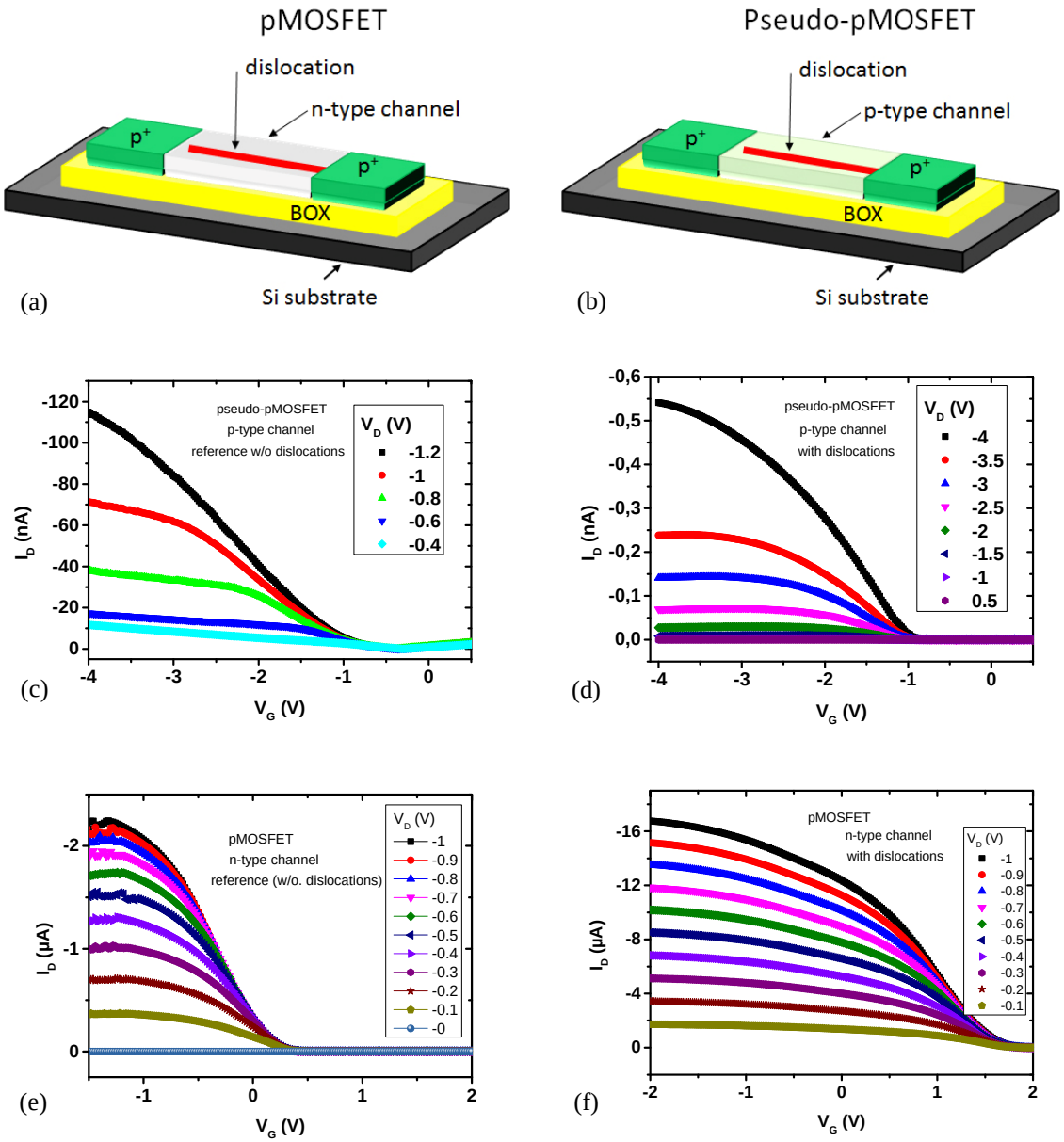

Fig. 6 Cartoon of a SOI pMOSFET (a) and a pseudo-pMOSFET (b). For pseudo-pMOSFETs low-doped p-type channels ($\rho \cong 8 \cdot 10^{14}$ at./cm^3) are used. Note that the source/drain doping (p$^+$) is about 10^{20} at/cm^3. Channels are the bonded wafer material in all cases without any implantation. Drain current (I_D) vs. gate voltage (V_G) for pseudo-pMOSFETs without (c) and with dislocations in the channel (d) and for pMOSFETs without (e) and with dislocations in the channel (f). Note the different scale

more is observed if dislocations are present in the channel (Figs. 6(a), (b)). The measured values of I_D are also lower by a factor of about 10^5 compared to data of equivalent nMOSFETs. In addition, also higher drain and gate voltages are required for measurements of pMOSFETs. This suggests

the suppression of the transport of holes via dislocations in *p*-type material. It can be assumed that electrons existing on dislocations (resulting in the increase of I_D for nMOSFETs) lead to a compensation of injected holes in the case of pMOSFETs. Furthermore, measurements on numerous devices refer to a different behavior of pMOSFETs prepared on varying *p*-type substrates containing dislocation networks of different dislocation types. Assuming the same conditions (V_G = -3.5V, V_D = -3V) a drain current of I_D = -2 nA is measured if only 60° dislocations are present, while only I_D = -0.5 nA is determined if screw dislocations are dominantly present in the channel.

Drain currents comparable to nMOSFETs are obtained if pMOSFETs without dislocations are realized in n-type material. A typical value of I_D is about 2 μA at $V_G = V_D$ = -1V (Fig. 6(c)). The introduction of dislocations into the channel of such pMOSFETs results in a further increase of I_D. The drain current reaches about 16 μA at $V_G = V_D$ = -1V, i.e., an increase by a factor of 8, which, however, is significantly smaller than for nMOSFETs. This means that there is an extra transport of holes via dislocations in *n*-type material. Because the mobility of holes in silicon is lower than for electrons, the increase of the drain current in n-type material is lower than in *p*-type material. This interpretation is confirmed by device simulations of pMOSFETs showing that not only the concentration of carriers is important (as in the case of the nMOSFETs). Instead, a simultaneous increase of the hole mobility is also required to interpret the measured data of pMOSFETs. All these experimental data refer to different electronic properties of dislocations in *n*-type material compared to such defects in *p*-type material. It can be stated that a dislocation in *p*-type silicon forms an efficient one-dimensional channel for electrons, while a dislocation in *n*-type material causes a one-dimensional channel for holes. A more detailed discussion on the base of the band structure is given elsewhere (Kittler *et al*. 2013).

5. Conclusions

The embedding of two-dimensional configurations of well-defined numbers and types of dislocations into channels of MOSFETs is eminently suited to analyse the electrical properties of only a few or individual dislocations.

A method to realize defined arrangements of dislocations in a reproducible way is hydrophobic wafer bonding. Two-dimensional dislocation networks are produced if two wafers are bonded. The length and distance of the dislocations in a network is defined by the mesh size and can be up to several micrometers. Combining wafer bonding with pattern formation techniques (photolithography and dry etching) devices were realized allowing the measurement of the electrical properties of only a few dislocations.

Measurements of the characteristics of MOSFETs refer to an ambipolar character of dislocations in silicon. Devices prepared in *p*-type material show an increase of the drain current by more than one order of magnitude for nMOSFETs while a decrease of I_D is found for pMOSFETs. This indicates that electrons are present on the core of dislocations in *p*-type material. Device simulations revealed about 200 electrons per micrometer dislocation length corresponding to a distance between free electrons of about 5 nm. The investigations refer to a metallic-like conductance along the dislocations caused by a two-dimensional carrier confinement.

An increase of the drain current was proved also for pMOSFETs fabricated in *n*-type material. This means that holes are transported via dislocations under these conditions. The increase of I_D, however, is smaller than for nMOSFETs in *p*-type material.

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